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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/893,598	06/29/2001	Yoshinori Uchiyama	01USFP644-M.K.	6524

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EXAMINER	
BELL, PAUL A	

ART UNIT	PAPER NUMBER
2675	

DATE MAILED: 10/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/893,598	UCHIYAMA, YOSHINORI	
	Examiner	Art Unit	
	PAUL A BELL	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *2/25/2004 AND 5/12/2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11-14* is/are allowed.

6)☒ Claim(s) *1-10 and 15-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-10, and 15-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With regard to claim 1, it is not clear how if n = > 2 that 2 < k< n because when n=2 how is it possible that k be both > 2 and also < 2 at the same time.

With regard to claim 15, it is not clear how if n = > 2 that 2 =< k< n because when n=2 how is it possible that k be both > = 2 and also < 2 at the same time.

With regard to claim 20, it is not clear how if n = > 2 that 2 = < k< n because when n=2 how is it possible that k be both > = 2 and also < 2 at the same time .

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 2 ,10, 15, 16, and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Takuwa (5,793,363).

With regard to claim 1 (as best understood in view of 112 2P) Takuwa teaches

a semiconductor circuit system comprising: a first signal line (figure 1, items Pst or Sck or DB) and n circuit sections (figure 1, items 1-1a, and 1-2a), where n is an integer equal to or more than 2, each of which includes an input terminal (figure 1, items ST or TIM or CK or D) and an output terminal (figure 1, items OUT1 and OUT2), wherein said input terminals of only predetermined k ones of said n circuit sections are connected to said first signal line (Pst also goes to TIM on 1-2a), where k is an integer satisfying 2<k<n, and said output terminal of an m-th one of said n circuit sections is connected to said input terminal of an (m+k)-th one of said n circuit sections, where (1 < m < n-k) (OUT1 in 1-1a goes to ST of 1-2a).

With regard to claim 2 Takuwa teaches the semiconductor circuit system according to claim 1, wherein each of said n circuit sections starts an operation in response to a start signal on said first signal line and stops the operation a predetermined time after the start of the operation (figure 3).

With regard to claim 10 Takuwa teaches the semiconductor circuit system according to claim 1, wherein said n circuit sections are respectively provided on different semiconductor chips (figure 1, item 1-1a, 1-2a, and 1-3a).

With regard to claim 15 (as best understood in view of 112 2P) Takuwa teaches A liquid crystal display apparatus, comprising: a liquid crystal display panel (figure 1, item 2); a horizontal drive unit (figure 1); and a vertical drive unit (figure 1 only illustrates the horizontal but it is essential to proper operation to have a vertical drive unit), wherein said horizontal drive unit further comprises: a first signal line (figure 1, items Pst or Sck or DB); and n circuit sections (figure 1, items 1-1a, and 1-2a)

where n is an integer equal to or greater than 2, each of which said n circuit sections has an input terminal (figure 1, items ST or TIM or CK or D) and an output terminal (figure 1, items OUT1 and OUT2), input terminals of only predetermined k ones of said n circuit sections are connected to said first signal line(Pst also goes to TIM on 1-2a),, where k is an integer satisfying 2=< k =< n, and said output terminal of an m*th one of said n circuit sections is connected to said input terminal of an (m + k)*th one of said n circuit sections, where 1 +< m = < n-k (OUT1 in 1-1a goes to ST of 1-2a).

With regard to claim 16 Takuwa teaches the apparatus according to claim 15, wherein each of said n circuit sections starts an operation in response to a start signal on said first signal line and stops the operation a predetermined time after the start of the operation (figure 3).

With regard to claim 20 (as best understood in view of 112 2P) teaches a method of reducing power consumption in a liquid crystal display device having a liquid crystal display panel with a horizontal drive unit and a vertical drive unit, wherein said horizontal drive unit comprises a first signal line and n circuit sections(figure 1, items 1-1a, and 1-2a), where n is an integer equal to or greater than 2, each of which said n circuit sections has an input terminal (figure 1, items ST or TIM or CK or D) and an output terminal (figure 1, items OUT1 and OUT2), said method comprising: connecting said first signal line to input terminals of only predetermined k ones of said n circuit sections(Pst also goes to TIM on 1-2a), where k is an integer satisfying 2=< k < n;

and connecting said output terminal of an m*th one of said n circuit sections to said input terminal of an (m+k)*th one of said n circuit sections, where 1 =< m =< n-k (OUT1 in 1-1a goes to ST of 1-2a).

Allowable Subject Matter

5. The following claims 1, 15 and 20 are drafted by the examiner and considered to distinguish patentably over the art used in the rejection in this application, the proposed claims 1, 15 and 20 are presented to applicant for consideration: If applicant amends claims as proposed it will require further consideration and/or search. These changes serve to clarify applicants claimed invention and also serve to overcome the 112 problems.

With regard to **claim 1** the disclosure teaches;

A semiconductor circuit system comprising: a first signal line; and n circuit sections where n is an integer variable equal to or more than ~~2~~ 4, each of which includes an input terminal and an output terminal, wherein said input terminals of only predetermined k ones of said n circuit sections are connected to said first signal line, where k is an integer ~~satisfying 2<k<n~~ variable equal to or more than 2, and said output terminal of an (m)th one of said n circuit sections is connected to said input terminal of an (m+k)th one of said n circuit sections, where ~~(1 < m < n-k)~~ m is an integer variable equal to or more than 1 and the largest possible value of m is where m is equal to less than the value of (n-k), wherein the n circuit sections are divided into g groups of k circuit sections each, where g is an integer variable equal to or more than 2, wherein n, the total number of circuit sections, is equal to g multiplied by k.

With regard to **claim 15** the disclosure teaches;

A liquid crystal display apparatus, comprising: a liquid crystal display panel; a horizontal drive unit; and a vertical drive unit, wherein said horizontal drive unit further comprises: a first signal line; and n circuit sections, where n is an integer variable equal to or greater than ~~2~~ 4, each of which said n circuit sections has an input terminal and an output terminal, input terminals of only predetermined k ones of said n circuit sections are connected to said first signal line, where k is an integer ~~satisfying 2=< k =< n~~ variable equal to or more than 2, and said output terminal of an (m)th one of said n circuit sections is connected to said input terminal of an (m + k)th one of said n circuit sections, where ~~1 =< m =< n-k~~ m is an integer variable equal to or more than 1 and the largest possible value of m is where m is equal to less than the value of (n-k), wherein the n circuit sections are divided into g groups of k circuit sections each, where g is an integer variable equal to or more than 2, wherein n, the total number of circuit sections, is equal to g multiplied by k.

With regard to **claim 20** the disclosure teaches;

A method of reducing power consumption in a liquid crystal display device having a liquid crystal display panel with a horizontal drive unit and a vertical drive unit, wherein said horizontal drive unit comprises a first signal line and n circuit sections, where n is an integer variable equal to or greater than ~~2~~ 4, each of which said n circuit sections has an input terminal and an output terminal, said method comprising: connecting said first signal line to input terminals of only predetermined k ones of said n circuit sections, where k is an integer ~~satisfying 2=< k =< n;~~ variable equal to or more than 2, and

connecting said output terminal of an (m)th one of said n circuit sections to said input terminal of an (m+k)th one of said n circuit sections, where ~~1 =< m =< n-k.~~ m is an integer variable equal to or more than 1 and the largest possible value of m is where m is equal to less than the value of (n-k), wherein the n circuit sections are divided into g groups of k circuit sections each, where g is an integer variable equal to or more than 2, wherein n, the total number of circuit sections, is equal to g multiplied by k.

With regard to the above claims 1, 15 and 20 for exemplary purposes only;

When k = 2	n can be equal to	4	and	g	will equal 2
as illustrated	n can be equal to	6	and	g	will equal 3
in figure 4	n can be equal to	8	and	g	will equal 4
	n can be equal to	10	and	g	will equal 5

When k = 3	n can be equal to	6	and	g	will equal 2
as illustrate	n can be equal to	9	and	g	will equal 3
in figure 10	n can be equal to	12	and	g	will equal 4
	n can be equal to	15	and	g	will equal 5

When k = 4	n can be equal to	8	and	g	will equal 2
	n can be equal to	12	and	g	will equal 3
	n can be equal to	16	and	g	will equal 4
	n can be equal to	20	and	g	will equal 5

6. With regard independent claims 1, 15 and 20 if amended as proposed will overcome applicants admitted prior art shown in figure 2 where all of the n circuits are connected to the "first signal line" wherein all of the circuits are activated at the same time consuming maximum power. Also the proposed amendments will overcome the used reference Takuma wherein only the first one of the n circuits are connected to the "first signal line" and each of the n circuit are activated by the proceeding circuit so as

to be sequentially activated wherein only one circuit is being activated at a time consuming the least power. In contrast applicant teaches a device that sequentially activates groups made up of 2 or 3 or 4 or 5 or 6 and so fourth, wherein the "first signal line" activates a first group and that first group puts out "a second signal" that activates the second group which continues the process down the line until all groups have been sequentially activated.

7. Claims 11-14 are allowed.

8. The following is a statement of reasons for the indication of allowable subject matter: The invention as claimed in applicant's independent claims 11 when considered as a whole, the exact arrangement of parts and/or the inter connections and functions, is not taught nor suggested by the prior art made of record. The prior art of record does not teach to summarize having; "a control circuit including a latch circuit, said control circuit connected with at least one of said plurality of register circuits as a specific register circuit and said plurality of differential input circuits....said specific register .....outputs a second signal to said latch circuit when the operation ends, and said control circuit activates said plurality of differential input circuits in response to a third signal to operate and stops the operations of said plurality of differential input circuits in response to said second signal", (as illustrated in figure 6, CONTROL CIRCUIT comprising items 11 (LATCH), 12 and 19 and signals D6 (first signal), D4 (second signal) and D1 (third signal)). The closest art of record is applicants own admitted prior art figure 3 which does not have the control circuit .

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Bell whose telephone number is (703) 306-3019. If attempts to reach the examiner by telephone are unsuccessful the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377 can help with any inquiry of a general nature or relating to the status of this application.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

Or Faxed to: (703) 872-9306
Or Hand-delivered to: Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Paul Bell
Art unit 2675
October 18, 2004

REGINA LIANG
PRIMARY EXAMINER